

REMARKS

In an Office Action mailed on August 22, 2002, objections were made to the drawings; an objection was made to the specification; an objection was made to claim 16; claim 22 was rejected under 35 U.S.C. § 112, first paragraph; claims 1-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over alleged Applicant's admitted prior art ("AAPA") in view of Tjandrasuwita; and claim 16 was rejected under 35 U.S.C. § 103(a) as being unpatentable over alleged AAPA in view of Tjandrasuwita and in view of Sproch.

Amendments have been made to the specification and to the drawings to overcome most of the objections to the drawings. The remaining objections to the drawings are discussed in the corresponding section below. Claim 16 has been amended to overcome the corresponding objection to claim 16. The specification has been amended to address some of the objections to the specification, with the objection to the specification not having a brief Summary of the Invention section being discussed in the corresponding section below. The §§ 112 and 103 rejections are discussed in the corresponding sections below.

Remaining Objections to the Drawings:

The Examiner made an objection to the drawings because "reference character '14' has been used to designate both cell and double pumped bus system." Office Action, p. 2. However, Applicant does not understand the basis for this rejection. In other words, Applicant cannot find where in the drawings or specification that the character "14" is used to designate both a cell and double pumped bus system. Thus, without a more specific basis for this objection, withdrawal of this objection is requested.

The drawings were objected to because the drawings allegedly do not contain the reference sign "10," a reference sign mentioned on line 22 of page 1. However, Applicant submits that the reference sign 10 is depicted at the top right hand corner of Fig. 1. Therefore, withdrawal of this objection is requested.

The Examiner makes the following objection: "the timing diagram in Fig. 4 through Fig. 8 is incorrect in light of the specification." Applicant does not understand the basis for this objection without more specific reasons from the Examiner. It is assumed that this objection is made due to the required renumbering of Figs. 4-8 into one figure number. This requirement has

been satisfied as Figs. 4-8 have been incorporated into Fig. 3. Thus, withdrawal of this objection is requested.

The Examiner objects to the drawings because there is allegedly not a reference sign 168 in Fig. 10. However, Applicant submits that there is such a reference sign. In this manner, the reference sign "168" is depicted on the right hand side of Fig. 10 (now Fig. 5) as being a node between the output terminal of a pass gate 172 and the output terminal of the pass gate 174. Therefore, withdrawal of this objection is requested.

Objection to the Specification for Not Including a Brief Summary of the Invention:

The Examiner objects to the specification because it lacks a Summary of the Invention section. However, Applicant respectfully traverses this objection. In this manner, it is clear from the language of the regulations which sections of the specification are mandatory and which are permissive. For example, 37 C.F.R. § 1.27(b) requires: "a brief abstract of the technical disclosure in the specification which **must** commence on a separate sheet, preferably following the claims, under the heading 'Abstract of the Disclosure.'" In similar fashion, 37 C.F.R. § 1.75(a) states: "The specification **must** conclude with a claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention or discovery." In contrast, 37 C.F.R. § 1.73 states "a brief summary of the invention indicating its nature and substance, which may include a statement of the object of the invention, **should** precede the detailed description," and further states, "such summary **should, when set forth**, become commensurate with the invention as claimed."

Accordingly, it is submitted that a Summary of the Invention section is not required, and thus, Applicant respectfully declines to submit one.

Rejections of Claims 1-14:

The apparatus of claim 1 and the computer system of claim 10 each includes a first circuit to receive indications of first data that is associated with a first data set and second data that is associated with a second data set. The apparatus of claim 1 and the computer system of claim 10 also each includes a second circuit that is coupled to the first circuit. The second circuit causes the first circuit to in a first mode, communicate indications of the first data to an output terminal in synchronization with a first phase of a clock signal and communicate indications of the second

data to the output terminal in synchronization with a second phase of the clock signal. In a second mode, the second circuit causes the first circuit to communicate the indications of the first data to the output terminal in synchronization with the first phase and prevent communication of the second data during the second phase.

The Examiner fails to establish a *prima facie* case of obviousness for claims 1 and 10. In this manner, the Examiner combines the alleged admitted prior art with Tjandrasuwita in an attempt to establish a case of obviousness and particularly refers to Fig. 5. However, Tjandrasuwita does not supply the limitations that are missing from the alleged admitted prior art, as Tjandrasuwita teaches disabling a clock signal to a latch circuit 502. Disabling the latch circuit 502 prevents the communication of all data, not the disabling of a particular phase of a clock signal to disable communication of the second set of data. Thus, Tjandrasuwita does not disclose the missing claim limitations and in fact, teaches away from the claimed invention. Therefore, for at least this reason, a *prima facie* case of obviousness for either claims 1 or 10 has not been established.

Furthermore, a *prima facie* case of obviousness has not been established for the additional reason that the Examiner provides no support for a suggestion or motivation for the combination. In this manner, the Examiner must specifically point out such a suggestion or motivation in the prior art. *Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143. This requirement has not been met by the Examiner. As obviousness cannot be predicated on what is unknown, a *prima facie* case of obviousness has not been established for at least this additional reason. *In re Spormann*, 363 F.2d 444, 448, 150 USPQ 449, 452 (CCPA 1966).

Thus, for at least the reason that a *prima facie* case of obviousness has not been established for independent claims 1 and 10, withdrawal of the rejections of claims 1-14 is requested.

Rejections of Claims 15-19:

The system of claim 15 includes double pumped bus circuit serially coupled together to form a chain to communicate data from at least two different sets of data. At least one of the bus circuits is capable of being disabled to prevent bits from at least one of the sets of data from being communicated through the bus circuit.

Claim 15 is patentable for at least the reason that the Examiner fails to establish a *prima facie* case of obviousness. In this manner, the Examiner must show specific support for a suggestion or motivation to combine Tjandrasuwita with the alleged admitted prior art. Otherwise, a *prima facie* case of obviousness has not been established. Furthermore, Tjandrasuwita teaches away from claim 15, as Tjandrasuwita teaches disabling the communication of all data.

Thus, for at least these reasons, a *prima facie* case of obviousness has not been established for claim 15, and withdrawal of the rejections of claims 15-19 is requested.

Rejections of Claims 20-23:

The method of claim 20 includes receiving first indications of first data that is associated with a first data set. The method also includes receiving second indications of second data that is associated with a second data set. In a first mode, the first indications are communicated to a double pumped bus in synchronization with a first phase of a clock signal, and the second indications are communicated to the double pumped bus in synchronization with a second phase of the clock signal. In the second mode, the method includes communicating the first indications to the double pumped bus in synchronization with the first phase and preventing communication of the second indications to the double pumped bus during the second phase.

The Examiner fails to establish a *prima facie* case of obviousness for claim 20. In this manner, the Examiner provides no support for a suggestion or motivation to combine Tjandrasuwita with alleged admitted prior art. Furthermore, Tjandrasuwita teaches disabling all communications, not disabling a data state associated with one phase and allowing communications to proceed with another phase. Thus, for at least this additional reason, the Examiner fails to establish a *prima facie* case of obviousness for claim 20.

Thus, for at least the reason that a *prima facie* case of obviousness has not been established for claim 20, withdrawal of the rejections of claims 20-23 is requested.

CONCLUSION

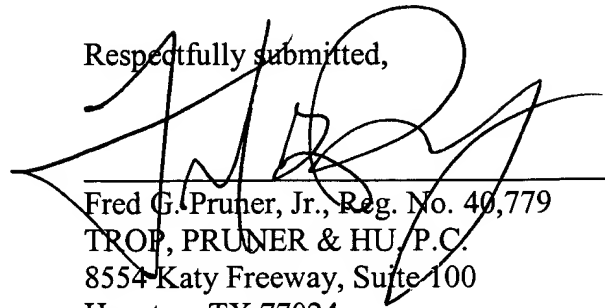
In view of the foregoing, withdrawal of the rejections and objections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to

charge any additional fees or credit any overpayment to Deposit Account No. 20-1504
(ITL.0349US).

Date: _____

8/29/02

Respectfully submitted,



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PATENT TRADEMARK OFFICE



SPECIFICATION AMENDMENTS

The paragraph beginning on line 1 of page 3 has been rewritten as follows:

Referring to Fig. 2, several cells 12 and 14 (cells 14a, 14b and 14c, as examples) may be serially coupled together to form a chain to relay data between the cells 14 using the double pumped technique that is described above. In this manner, the cell 12 is the first in the chain, and the cells 14 precede the cell 12 in the chain. As an example, Fig. 3 depicts [Figs. 6, 7 and 8 depict] signals called DP1, DP2 and DP3 that are furnished by the cells 12, 14a and 14b, respectively, and illustrate the propagation of data bits between the cells 12 and 14. For example, referring to Fig. 3 [Figs. 3, 4 and 5], the CLK signal [(see Fig. 3)] has a negative edge at time T_1 , and in response to this negative edge, the cell 12 latches a bit (represented by the portion 50 of the DATA1 signal) for the first data set. At time T_2 , the CLK signal has a positive edge, an edge that causes the cell 12 to latch a bit (represented by the portion 52 [50] of the DATA2 signal) for the second data set. After time T_1 during the logic zero state of the CLK signal, the cell 12 begins furnishing the bit 50 to the cell 14a. It is noted that the bit 50 may not appear until after a slight propagation delay, as depicted in Fig. 3 [5]. After time T_2 during the logic one state of the CLK signal, the cell 12 begins furnishing the bit 52 to the cell 14a, as depicted in Fig. 3 [6]. The cells 14a and 14b then relay the bits 50 and 52 in a time multiplexed fashion [as depicted in Figs. 7 and 8].

The paragraph beginning on line 25 of page 3 has been rewritten as follows:

Fig. 3 depicts [Figs. 3, 4, 5, 6, 7 and 8 are] waveforms illustrating signals of the double pumped bus system of Fig. 2.

The paragraph beginning on line 27 of page 3 has been rewritten as follows:

Figs. 4 [9] and 6 [11] are schematic diagrams of double pumped bus cells according to embodiments of the invention.

The paragraph beginning on line 29 of page 3 has been rewritten as follows:

Fig. 5 [10] is a more detailed schematic diagram of the cell of Fig. 4 [9] according to an embodiment of the invention.

The paragraph beginning on line 1 of page 4 has been rewritten as follows:

Fig. 7 [12] is a schematic diagram of a double pumped bus cell system according to an embodiment of the invention.

The paragraph beginning on line 3 of page 4 has been rewritten as follows:

Fig. 8 [13] is a schematic diagram of a computer system according to an embodiment of the invention.

The paragraph beginning on line 7 of page 4 has been rewritten as follows:

Referring to Fig. 4 [9], an embodiment 100 of a double pumped bus cell in accordance with the invention may be set up to communicate either one or two sets of data. More specifically, in some embodiments of the invention, an EN signal that is received by the cell 100 may be asserted (driven high, for example) to enable the cell 100 to latch, store and retransmit bits of data from two different data sets in a time multiplexed fashion. In this manner, a data line 107 communicates a signal (called DATAIN) that indicates bits of data from a first data set and a second data set. The bits of the first data set are interleaved, or alternate, in time with the bits of the second data set.

The paragraph beginning on line 25 of page 5 has been rewritten as follows:

To accomplish the above-described features, in some embodiments of the invention, the cell 100 may include logic, such as an AND gate 112, that receives the CLK and EN signals. The output terminal of the AND gate 112 is coupled to the inverting clock input terminal of the bit latch 104, and the clock input terminal of the bit latch 102 [106] receives the CLK signal. Because the bit latches 102 and 104, in some embodiments of the invention, invert the logic levels of the stored bits, the cell 100 may include an inverter 108 that is coupled between the data input line 107 and the input terminals of the bit latches 102 and 104. When the EN signal is de-asserted, the output terminal of the AND gate 112 is de-asserted, regardless of the logic level of the CLK signal, and thus, the bit latch 104 does not store any new data as long as the EN signal remains de-asserted. However, when the EN signal is asserted, the CLK signal controls the signal at the output terminal of the AND gate 112 and thus, controls the reception of data into the bit latch 104.

The paragraph beginning on line 6 of page 6 has been rewritten as follows:

Fig. 5 [10] depicts a more detailed schematic diagram of the cell 100 in accordance with some embodiments of the invention. As shown, the bit latch 102 may include a circuit 140 that is effectively a complementary metal oxide semiconductor (CMOS) inverter that is enabled when the CLK signal (that alternates between logic one and logic zero states) is in a logic one state to latch the bit that is indicated by the DATAIN signal. To accomplish this, the circuit 140 includes an n-channel metal-oxide-semiconductor field-effect-transistor (NMOSFET) 148 that has its source terminal coupled to ground and its drain terminal coupled to the source terminal of another NMOSFET 146. The drain terminal of the NMOSFET 146 is coupled to the drain terminal of a p-channel metal-oxide-semiconductor field-effect-transistor (PMOSFET) 144. The source terminal of the PMOSFET 144 is coupled to the drain terminal of another PMOSFET 142, and the drain terminal of the PMOSFET 142 is coupled to a positive voltage supply level (called V_{DD}). The gate terminals of the PMOSFET 144 and the NMOSFET 146 respond to the logical state of the CLK signal to control when the circuit 140 is enabled. In this manner, the gate terminal of the PMOSFET 144 is coupled to a clock input terminal 131 (that furnishes the CLK signal) via a chain 124 of three serially coupled inverters 240 that invert the CLK signal to receive an inverted version of the CLK signal. The gate terminal of the NMOSFET 146 is coupled to a chain 123 of serially coupled inverters 120 to the clock line 131 to receive an indication of the CLK signal. The gate terminals of the PMOSFET 142 [144] and the NMOSFET 148 are coupled to the data input line 107.

The paragraph beginning on line 5 of page 7 has been rewritten as follows:

Similar to the bit latch 102, the bit latch 104 includes the circuit 140 and the bit latch that is formed from inverters 160 and 162. However, unlike the bit latch 102, the gate terminals of the circuit 140 of the bit latch 104 [140] are connected differently. In this manner, the gate terminal of the PMOSFET 144 is coupled to the output terminal of a NAND gate 124, and the gate terminal of the NMOSFET 146 is coupled to the output terminal of an inverter 136 that has its input terminal coupled to the output terminal of the NAND gate 124. One input terminal of the NAND gate 124 is coupled between the inverter 120 to receive an inverted indication of the CLK signal, and the other input terminal of the NAND gate 124 is coupled to an enable input line 113 to receive the EN signal. Thus, when the EN signal is asserted, the circuit 140 of the bit latch 104 is enabled during the logic zero state of the CLK signal to update the bit that is stored

by the inverters 160 [166] and 162 [168] of the circuit 104 [140]. During the logic one state of the CLK signal and when the EN signal is de-asserted, the circuit 140 is disabled. Thus, when the CLK signal transitions from the logic zero to the logic one state on a positive edge, the CMOS inverter becomes disabled to latch the bit that is stored in the inverters 160 and 162 of the bit latch 104.

The paragraph beginning on line 20 of page 7 has been rewritten as follows:

In some embodiments of the invention, the multiplexer 106 includes two CMOS pass gates 172 and 174. The input terminal of the CMOS pass gate 172 is coupled to the output terminal of the inverter 164 of the bit latch 102, and the output terminal of the CMOS pass gate 172 is coupled to a node 168 that forms the output terminal of the multiplexer 106. The inverting control, or selection, terminal of the pass gate 172 is coupled to the gate terminal of the NMOSFET 146 of the bit latch 102, and the non-inverting control, or selection, terminal of the pass gate 172 is coupled to the gate terminal of the PMOSFET 144 of the bit latch 102. Thus, due to this arrangement, the output terminal of the bit latch 102 is coupled to the output terminal of the multiplexer 106 [160] when the CLK signal has a logic zero level. The input terminal of the CMOS pass gate 174 is coupled to the output terminal of the inverter 164 of the bit latch 104, and the output terminal of the CMOS pass gate 174 is coupled to the node 168. The inverting control terminal of the pass gate 174 is coupled to the non-inverting control terminal of the pass gate 172, and the non-inverting control terminal of the pass gate 174 is coupled to the inverting control terminal of the pass gate 172. Thus, due to this arrangement, the output terminal of the bit latch 104 is coupled to the output terminal of the multiplexer 106 [160] when the CLK signal has a logic one level. In some embodiments of the invention, the inverter 110 may include a chain of three inverters 109 that are coupled between the node 168 and the output terminal 170.

The paragraph beginning on line 7 of page 8 has been rewritten as follows:

The cell 100 that is described above receives time-multiplexed bits of data from a single wire. However, in some embodiments of the invention, a cell 200 that is depicted in Fig. 6 [11] may be used in place of the cell 100. The cell 200 has a similar design to the cell 100 except for the following features. Unlike the cell 100, the cell 200 has two data input lines 203 and 205 (instead of one) to receive bits of data from circuits that are associated with two different data sets. In this manner, the inverter 108 (see Fig. 4 [9]) of the cell 100 is replaced by two inverters

202 and 207 of the circuit 200. The input terminal of the inverter 202 receives a signal (called DATA1) that is indicative of bits of data from the first data set, and the input terminal of the inverter 207 receives a signal (called DATA2) that is indicative of bits of data from the second data set. The output terminal of the inverter 202 is coupled to the data input line of the bit latch 102, and the output terminal of the inverter 207 is coupled to the data input line of the bit latch 104.

The paragraph beginning on line 19 of page 8 has been rewritten as follows:

Referring to Fig. 7 [12], in some embodiments of the invention, the cells 100 (the enabled cells 100a and the disabled cells 100b, as described below) and 200 may be used to form a double pumped bus chain 220 for purposes of communicating the bits of data from the first and second data sets across an integrated circuit, for example. In this manner, the cell 200 is the first in the chain 220 to arrange bits from the two different data sets in a time interleaved fashion. The cells 100 may be serially coupled together after the cell 200. As shown, to disable the flow of the bits of the data set that is associated with the DATA2 signal, every other cell 100 is disabled, as depicted in Fig. 7 [12] by the enabled cells 100a and the disabled cells 100b. This alternative disabling of the cells 100 occurs because each cell 100 reverses the phasing of the data flow. For example, each cell 100 receives the bits of a particular data set on positive clock edges and retransmits the bits of that data set on negative clock edges. The arrangement that is depicted in Fig. 7 [12] is used to disable the flow of bits for the data set that is associated with the DATA2 signal. However, alternatively, to disable the bits for the data set that is associated with the DATA1 signal, the enable input terminals 113 of the cells 200 and 100b are asserted, and the enable input terminals 113 of the cells 100a are de-asserted.

The paragraph beginning on line 4 of page 9 has been rewritten as follows:

Referring to Fig. 8 [13], as an example, the cell 200 (and/or the cell 100) may be used in a semiconductor circuit, such as a processor 252 (a microprocessor, such as a Pentium® microprocessor, as an example), to communicate bits of data between circuits 254, 256, 260 and 262 of the processor 252. In this manner, the cell 200 may communicate data over a wire 258 for two data sets. More specifically, the cell 200 may communicate data for a first data set between the circuit 254 that is located at one end of the wire 258 and the circuit 260 that is located at another end of the wire 268. The cell 200 may also communicate data for a second

data set between the circuit 256 that is located at one end of the wire 258 and the circuit 262 that is located at the other end of the wire 268.

CLAIM AMENDMENTS:

The claims have been amended as follows:

16. (Amended) The system of claim 15, wherein alternate double pumped circuits are disabled to prevent the bits from at least one of the sets of data from [form] being communicated through said at least one of the bus circuits.

22. (Amended) The method of claim 20, wherein the receiving the second indications comprises:

latching the second indications one bit at a time in response to the first mode.